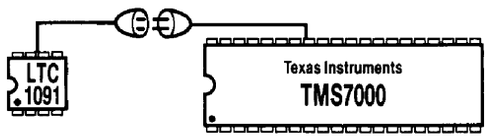
Interfacing the LTC1091 to the TMS7742 MCU



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Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the TMS7000 family of microcomputers (e.g., TMS7742). The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the TMS7742 in 99μs. Configuration of the LTC1091 and the TMS7742 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous, half duplex format over D_{IN} and D_{OUT}.

The TMS7742 contains a synchronous, full duplex, serial port that allows the user to construct a simple communication path to the LTC1091. The serial port provides clock, transmit and receive lines that are compatible with the LTC1091. The only additional line required is one programmable output pin (A0) to control $\overline{CS}$ on the LTC1091.

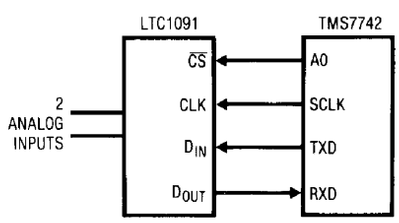

Figure 1. Schematic

The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The TMS7742 was chosen because it contains 4k of EPROM which can be programmed using a standard EPROM programmer. Any member of the TMS7000 family which contains a serial port should be able to use this code with only modifications to the peripheral register numbers.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. The TMS7742 clock was 5 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

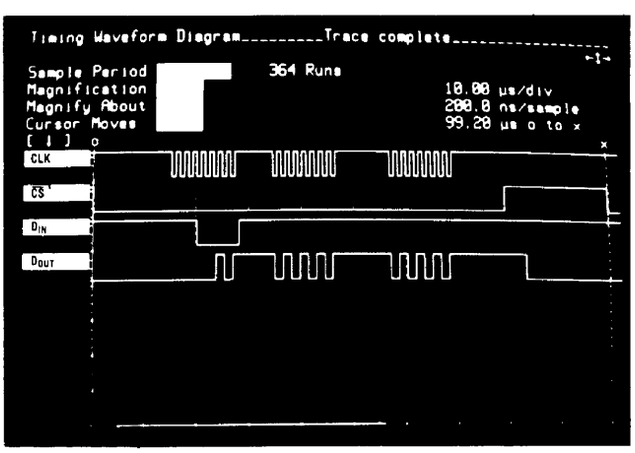

Figure 2. Timing Diagram

Software Description

The software configures and controls the serial port of the TMS7742. Additionally, the software manipulates A0 ($\overline{CS}$ of the LTC1091).

The code first disables all interrupts and initializes the stack. The data direction register for the A port then sets A5 (RXD) as an input and all other bits including A0 ($\overline{CS}$) as outputs. Next the serial port is configured. Tx is enabled, the serial port is reset, and the SMODE register is configured for 8 bits, no parity, and one stop bit. The SCLK rate is set to the processor clock frequency divided by 4.

The SCLK is turned off and A0 ($\overline{CS}$) is cleared. The D_{IN} word of the LTC1091 is loaded into the TXBUF. This D_{IN} word (07) configures the LTC1091 for CH1 with respect to ground and LSB first. Examine Figure 3 to see how this is constructed keeping in mind that the TMS7742 transmits data LSB first. The serial port and SCLK are turned on and the data is shifted while the processor idles in a loop. The first eight bits contain the D_{IN} word and the first three MSBs of the D_{OUT} word. (The LTC1091 clocks out the data MSB first and then LSB first when in the LSB first mode.) The serial port is turned on again and the next eight bits containing the rest of the MSB first data and the first two bits of the LSB first data are shifted while the processor idles in a loop. The data containing the LSBs is then placed in the B register. The procedure is repeated for the next eight bits which contain the MSBs and the result is placed in the A register. A0 ($\overline{CS}$) is then set. The data in the B register is stored in R5. If desired the lowest six bits of the B register can be cleared by adding them with $C0. The data in the A register is stored in R6. The data is now stored left justified as shown in Figure 4.

0	0	0	0	0 MSBF	1 O/S	1 S/D	1 START	P23

Figure 3. D_{IN} Word for LTC1091 Stored in TMS7742 TXBUF

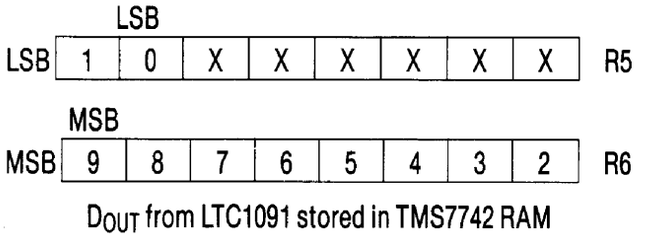

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
START	DINT		DISABLES ALL INTERRUPTS
	MOVP	%>2A,P0	DISABLE INTERRUPT FLAGS
	MOVP	%>02,P16	DISABLE INTERRUPT FLAGS
	MOV	%>60,B	ADDRESS OF STACK
	LDSP		PUT ADDRESS INTO POINTER
	MOVP	%>DF,P5	CONFIGURE PORT A
	MOVP	%>08,P6	ENABLE Tx BY SETTING B3 = 1
	MOVP	%>00,P17	P17 POINTS TO SCTL0
	MOVP	%>40,P17	RESET THE SERIAL PORT
	MOVP	%>0C,P17	CONFIGURE THE SERIAL PORT
	MOVP	%>00,P21	TURN START BIT OFF
	MOVP	%>00,P17	ENABLE THE SERIAL PORT
	MOVP	%>00,P20	SET SCLK RATE (TIMER 3)
LOOP	MOVP	%>40,P21	SCLK OFF
	ANDP	%>FE,P4	A0 CLEARED ($\overline{CS}$ GOES LOW)
	MOVP	%>07,P23	PUT LTC1091 D_{IN} INTO TXBUF
	MOVP	%>17,P17	ENABLE SERIAL PORT
	MOVP	%>C0,P21	SCLK ON (TRANSFER BEGINS)
	MOVP	%>14,P17	TXEN GOES LOW
	MOV	%>02,A	LOAD COUNTER
WAIT	DJNZ	A,WAIT	LOOP WHILE SHIFT OCCURS
	NOP		MORE DELAY
	MOVP	%>17,P17	ENABLE SERIAL PORT
	MOVP	%>14,P17	TXEN GOES LOW
	MOV	%>02,A	LOAD COUNTER
WAIT1	DJNZ	A,WAIT1	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P22,B	PUT D_{OUT} FROM LTC1091 IN B
	MOVP	%>17,P17	ENABLE SERIAL PORT
	MOVP	%>14,P17	TXEN GOES LOW
	MOV	%>02,A	LOAD COUNTER
WAIT2	DJNZ	A,WAIT2	LOOP WHILE SHIFT OCCURS
	NOP		DELAY
	MOVP	P22,A	PUT D_{OUT} FROM LTC1091 IN A
	ORP	%>01,P4	A0 SET ($\overline{CS}$ GOES HIGH)
	MOV	B,R5	PUT FIRST 2 LSBs IN R5
	MOV	A,R6	PUT MSBs IN R6

Figure 5. TMS7742 Code

Summary

A four wire interface between the LTC1091 and the TMS7742 with a combined data conversion and transfer time of 99μs was demonstrated. The interface used the serial port of the TMS7742. Because the serial port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1091. The 10 data bits of the LTC1091 are shifted LSB first in three eight bit transfers. The data is stored left justified in the TMS7742's internal RAM.